PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG-IPC/14/8713
Dated 02 Oct 2014

HBIP40 Technology for Voltage reference TL1431

Table 1. Change Implementation Schedule

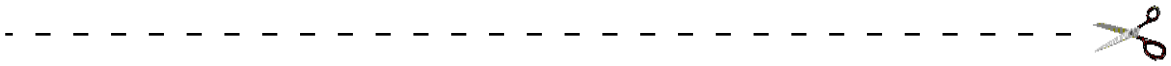
Forecasted implementation date for change	19-Dec-2014
Forecasted availability date of samples for customer	25-Sep-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	25-Sep-2014
Estimated date of changed product first shipment	01-Jan-2015

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Product design change
Reason for change	This manufacturing change will improve service to ST Customers
Description of the change	Following Divisional Commitments towards a continuous improvement philosophy, a more fine geometry Bipolar Technology called HBIP40 has been qualified in ST. ST is going to use this improved technology to redesign the Voltage Reference TL1431. The present PCN notifies the fully qualification of TL1431AC and TL1431C devices. Quality and electrical performances are guaranteed
Change Product Identification	Digit "H" is marked on the physical parts, on the string after P/N marking
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPG-IPC/14/8713**
Please sign and return to STMicroelectronics Sales Office	**Dated 02 Oct 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Riviera, Antonio	Marketing Manager
Naso, Lorenzo	Product Manager
Moretti, Paolo	Q.A. Manager

WHAT:

Following Divisional Commitments towards a continuous improvement philosophy, a more fine geometry Bipolar Technology called HBIP40 has been qualified in ST. ST is going to use this improved technology to redesign the Voltage Reference TL1431. The present PCN notifies the fully qualification of TL1431AC and TL1431C devices. Quality and electrical performances are guaranteed.

For the complete list of the part numbers affected by the change, please refer to the attached Products list.

WHY:
New equipment utilization, capacity optimization.
This manufacturing change will improve service to ST Customers.

HOW:
The qualification program mainly consist of reliability tests and comparative electrical characterizations.
The related reliability report is annexed to this document.
The changes here reported do not affect the electrical, dimensional and thermal parameters of the products, keeping unchanged all information reported on the relevant datasheets.

WHEN:

Te implementation will be finalized within Week 50-14

Marking and traceability:

Digit “H” is marked on the physical parts, on the string after P/N marking.

The changed here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.
There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change.
After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer’s written agreement.

Reliability Report

Voltage References

New Products

TL1431AC & TL1431C

Technology HBIP40V
Package: SO8 & SOT23-3L

General Information	
Product Line	M43101
Product Description	Programmable voltage reference
P/N	TL1431ACDT TL1431ACL3T
Product Group	IPG IPC
Product division	Linear Voltage Regulators & Vref
Packages	SO8 SOT23
Silicon Process technology	HBIP40V

Locations	
Wafer fab	*AMK6*
Assembly plant	*SHENZHEN (SO8)* *CARSEM (SOT23-3L)*
Reliability Lab	*CATANIA*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	Jun-2013	8	Giuseppe Failla	Giovanni Presti	Final report

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
AECQ100	Failure mechanism based stress test qualification for integrated circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

New products qualification: TL1431ACDT & TL1431ACL3T diffused in technology HBIP40 in SO8 and SOT23 packages.

3.2 Conclusion

The present reliability evaluation is considered positive with reference to the product versions “C” and “AC”, having at datasheet operating temperature from -20°C to 70°C.

4 DEVICE CHARACTERISTICS

4.1 Device description

The TL1431 is a programmable shunt voltage reference with guaranteed temperature stability over the entire operating temperature range.The output voltage may be set to any value between 2.5 V and 36 V with two external resistors.
The TL1431 operates with a wide current range from 1 to 100 mA with a typical dynamic impedance of 0.2 Ω.

4.2 Construction note

P/N	TL1431ACDT	TL1431ACL3T
	SO8	SOT23-3L
Wafer/Die fab. information		
Wafer fab manufacturing location	SINGAPORE Ang Mo Kio	
Technology	HBIP40V	
Die finishing back side	Lapped Silicon	
Die size	830, 780 micron	
Passivation type	PVAPOX/NITRIDE	
Wafer Testing (EWS) information		
Electrical testing manufacturing location	Ang Mo Kio EWS	
Tester	ASL1000	
Test program	M431_AFTER_ESI.nx4	
Assembly information		
Assembly site	SHENZHEN B/E	CARSEM M
Package description	SO 08 .15 JEDEC	SOT 23 3 LDS
Molding compound	Epoxy	epoxy
Frame material	NiThPdAgAu	HDLF NiPdAu
Die attach material	Epoxy	Epoxy
Wires bonding materials/diameters	1 mils CU Wire	
Final testing information		
Testing location	SHENZHEN B/E	CARSEM S
Tester	ASL1000	
Test program	M431_STS_01.nx4	M431_1

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	SO8	M43101	
2	SOT23-3L (grade 3)	M43101	

5.2 Test plan and results summary

P/N TL1431ACDT_ TL1431ACL3T

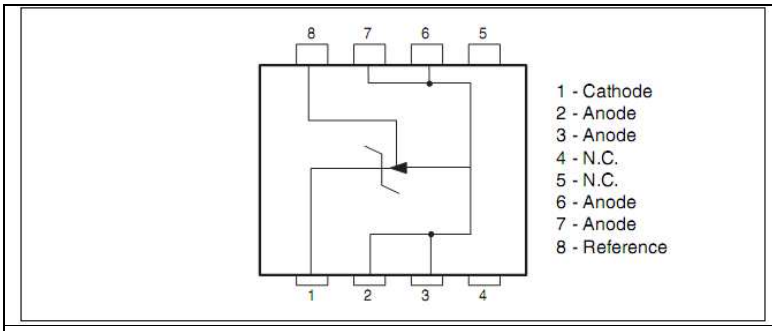
Test	PC	Std ref.	Conditions		Steps	Failure/SS		Note
						SO8	SOT23-3L	
Die Oriented Tests								
HTOL	N	JESD22 A-108	Ta = 85°C, BIAS +5V		168 H	0/77	0/77	
					500 H	0/77	0/77	
					1000 H	0/77	0/77	
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/45	0/45	
					500 H	0/45	0/45	
					1000 H	0/45	0/45	
Package Oriented Tests								
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	Pass	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	0/77	0/77	
TC	Y	JESD22 A-104	Ta = -40°C to 125°C		100 cy	0/77	0/77	
					200 cy	0/77	0/77	
					500 cy	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH=85%, BIAS +2.8V		168 H	0/77	0/77	
					500 H	0/77	0/77	
					1000 H	0/77	0/77	
Other Tests								
ESD	N	AEC Q101-001, 002 and 005	HBM	3	2KV	Pass		
			CDM	3	1.5KV	Pass		
			MM	3	200V	Pass		

Product grade 3

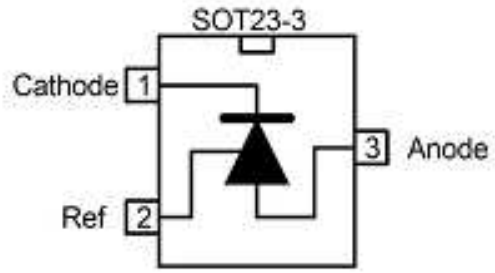
6 ANNEXES

6.1 Device details

6.1.1 Pin connection

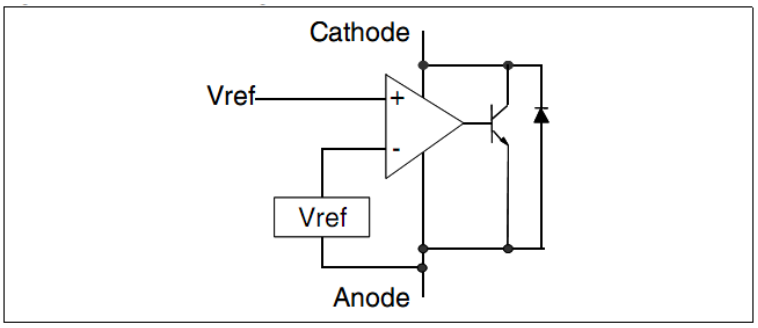


SO8



SOT23-3L

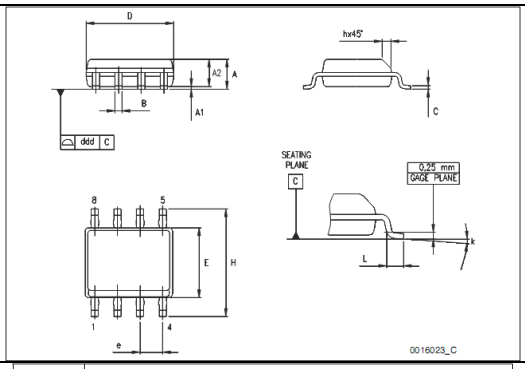
6.1.2 Block diagram



6.1.3 Package outline/Mechanical data

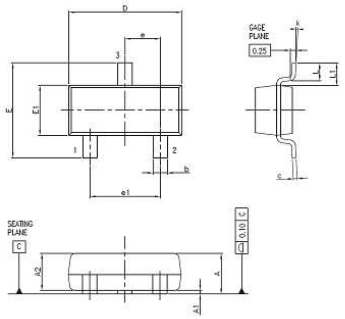
SO8 / SOT23-3L package information

SO8



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	1°		8°	1°		8°
ccc			0.10			0.004

SOT23-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.89		1.12	0.035		0.044
A1	0.01		0.10	0.0004		0.004
A2	0.88	0.95	1.02	0.035	0.037	0.040
b	0.30		0.50	0.012		0.020
c	0.08		0.20	0.003		0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	2.10		2.64	0.083		0.104
E1	1.20	1.30	1.40	0.047	0.051	0.055
e		0.95			0.037	
e1		1.90			0.075	
L	0.40	0.50	0.60	0.016	0.020	0.024
L1		0.54			0.021	
k	0d		8d			

6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operative Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other Test		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CDM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.

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